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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/816,706
Filing Date: March 23, 2001
Appellant(s): CHOW, PETER KA-FAI

Robert A. Voigt, Jr. And Kelly K. Kordzik
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/21/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1 and 3-11.

Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Upon further reflection, Examiner finds that the prior art does not disclose or fairly suggest placing information in the LARQ header in a frame status frame which will follow the stripped frame. The prior art discloses that a frame that exceeds the maximum length for a network will be split into multiple frames. The prior art does not disclose or suggest where the split will occur or the types of information carried in each frame. Therefore, the prior art does not disclose placing the stripped LARQ information in a frame status frame, where the frame status frame is a particular type of frame. Examiner contacted Applicant's Representative on 6 July 2004, when this change to the status of the claims was made, in order to inform Applicant's Representative of the change in the status of the claims and to propose amendments

to the claims which would make the claims allowable. At that time, Applicant's Representative chose to continue with the appeal process.

(4) Status of Amendments After Final

The amendment after final rejection filed on 5/24/2004 has not been entered.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1 and 3 form a group and that claims 2 and 4-12 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,999,541	HINCHEY et al.	12-1999
6,335,933	MALLORY	1-2002
5,251,205	CALLON et al.	10-1993
WO 96/13106	GIBSON et al.	5-1996

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchey et al (USPN 5,999,541) in view of Mallory (USPN 6,335,933).

3. Regarding claims 1 and 5, Hinchey discloses a method and a line controller for modifying a packet to be compatible with a network, the method comprising the steps of and the controller comprising means for: (a) detecting a field in a frame (col. 1, line 66-col. 2, line 21); (b) stripping the field and a frame check sequence (FCS) in the frame (col. 1, line 66-col. 2, line 21; col. 5, lines 1-3; and col. 5, lines 4-28); (c) recalculating the FCS for the stripped frame (col. 1, line 66-col. 2, line 21; col. 5, lines 1-3; and col. 5, lines 4-28); and (d) adding the recalculated FCS to the stripped frame (col. 1, line 66-col. 2, line 21; col. 5, lines 1-3; and col. 5, lines 4-28). Hinchey does not disclose that the field is a limited automatic repeat request (LARQ) header. Mallory teaches, in an Ethernet network, modifying an Ethernet frame to include an LARQ header in order to reduce the effective error rate of an unreliable frame-based communication channel or network (col. 4, lines 16-38 and col. 6, lines 9-20). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have the field be an LARQ header in order to convert an Ethernet frame into an LARQ Ethernet frame and vice versa.

4. Regarding claim 3, referring to claim 1, Hinchey in view of Mallory implicitly discloses (e) sending the stripped frame with the recalculated FCS to an Ethernet controller (Hinchey: col. 1, line 66-col. 2, line 29, esp. col. 2, lines 22-29; col. 5, lines 1-3; and col. 5, lines 4-28) where an "Ethernet controller" is broadly defined as an Ethernet device capable of switching a packet.

5. Regarding claim 6, referring to claim 5, Hinchey in view of Mallory implicitly disclose that an asserted first signal to the first logic block indicates that the LARQ header is enabled and must be stripped from the frame. Although Hinchey in view of Mallory do not disclose the "nut and bolts" of the invention, it is implicit that a signal is needed to indicate that a packet translation is required.

6. Regarding claim 7, referring to claim 5, Hinchey in view of Mallory implicitly discloses that the first logic block asserts a second signal and a third signal to the second logic block, wherein the second signal indicates that the FCS is to be stripped from the frame, wherein the third signal indicates that the LARQ header is to be stripped from the frame. Although Hinchey in view of Mallory do not disclose the "nut and bolts" of the invention, it is implicit that signals are needed to indicate that a packet translation is required and how the translation is to be performed.

7. Regarding claim 8, referring to claim 5, Hinchey in view of Mallory implicitly discloses that an asserted fourth signal to the third logic block enables the recalculation of the FCS. Although Hinchey in view of Mallory do not disclose the "nut and bolts" of the invention, it is implicit that a signal is needed to indicate that new FCS should be calculated.

8. Claims 4 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hinchey et al (USPN 5,999,541) in view of Mallory (USPN 6,335,933) in further view of Gibson et al (WO 96/13106).

9. Regarding claim 4, referring to claim 3, Hinchey in view of Mallory does not expressly disclose (f) determining if a bit pattern at a set byte location in the stripped frame matches a wake pattern. Gibson teaches, in an Ethernet network, determining if a bit pattern at a set byte location in the stripped frame matches a wake pattern in order to remotely wake up a computer which is in sleep mode to save energy (page 6, lines 15-22; page 7, lines 14-19; and page 9, line 21-page 12, line 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to determine if a bit pattern at a set byte location in the stripped frame matches a wake pattern in order to remotely wake up a computer which is in sleep mode to save energy.

10. Regarding claim 9, Hinchey discloses a controller comprising: a first logic block for detecting a field in a frame (col. 1, line 66-col. 2, line 21), a second logic block for stripping the field and a FCS in the frame (col. 1, line 66-col. 2, line 21; col. 5, lines 1-3; and col. 5, lines 4-28), and a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame (col. 1, line 66-col. 2, line 21; col. 5, lines 1-3; and col. 5, lines 4-28). Hinchey does not disclose that the field is a limited automatic repeat request (LARQ) header. Mallory teaches, in a home phone Ethernet network, modifying an Ethernet frame to include an LARQ header in order to reduce the effective error rate of an unreliable frame-based communication channel or network (col. 4, lines 16-38 and col. 6, lines 9-20). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to have the field be an LARQ header in order to convert an Ethernet frame into an LARQ Ethernet frame and vice

versa such that the frame can be transmitted in a home phone network. Hinchey in view of Mallory does not expressly disclose that the system comprises an Ethernet controller in a sleep mode. Gibson teaches, in an Ethernet network, having Ethernet devices enter sleep mode in order to conserve power (page 6, lines 15-22; page 7, lines 14-19; and page 9, line 21-page 12, line 10). It would have been obvious to one of ordinary skill in the art at the time of the invention to have an Ethernet controller in a sleep mode such that the Ethernet controller conserves power.

11. Regarding claim 10, referring to claim 9, Hinchey in view of Mallory in further view of Gibson implicitly discloses that an asserted first signal to the first logic block indicates that the LARQ header is enabled and must be stripped from the frame. Although Hinchey in view of Mallory do not disclose the "nut and bolts" of the invention, it is implicit that a signal is needed to indicate that a packet translation is required.

12. Regarding claim 11, referring to claim 9, Hinchey in view of Mallory in further view of Gibson implicitly discloses that the first logic block asserts a second signal and a third signal to the second logic block, wherein the second signal indicates that the FCS is to be stripped from the frame, wherein the third signal indicates that the LARQ header is to be stripped from the frame. Although Hinchey in view of Mallory do not disclose the "nut and bolts" of the invention, it is implicit that signals are needed to indicate that a packet translation is required and how the translation is to be performed.

13. Regarding claim 12, referring to claim 9, Hinchey in view of Mallory in further view of Gibson implicitly discloses that an asserted fourth signal to the third logic block enables the recalculation of the FCS. Although Hinchey in view of Mallory do not disclose the "nut and

bolts" of the invention, it is implicit that a signal is needed to indicate that new FCS should be calculated.

(11) Response to Argument

On pages 6-7 of the Appeal Brief, Applicant argues that "Examiner has not presented any objective evidence for combining Hinchey and Mallory" since the "Examiner's motivation appears to have been gleaned from the secondary reference". Specifically, Applicant argues that one of ordinary skill in the art would not be motivated to combine a primary reference with a secondary reference when the primary reference does not contain an explicit motivation for the combination. Examiner disagrees with Applicant's assertion that the motivation provided in the secondary reference, Mallory, is insufficient to support a *prima facie* case of obviousness merely because this motivation is found in the secondary rather than the primary reference. Examiner submits that obviousness is not established by determining if one of ordinary skill in the art, after having read the primary reference, would have been motivated to find an additional reference to cure any defects in the primary reference given only the teachings of the primary reference, as Applicant suggests. Rather obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in *the references themselves* (not just the primary reference) or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Since motivation can only be determined "In light of all the evidence" (*In re Fine*), a proper case of *prima facie* obviousness can be made if the motivation is provided in the

secondary reference. In this case, the primary reference, Hinchey, teaches that "a first network packet having a header and an information field is prepared for transmission over a second network by the steps of removing the header information from the first network packet, and associating a second header with the information field of the first packet, wherein the second header is compatible with the second network" (col. 1, line 66-col. 2, line 21). Hinchey discloses, as the primary embodiment, that the first network is a Token Ring network and the second network is an Ethernet network; however, it is apparent from the wording of the above passage from Hinchey that this process can be applied to other network types. In addition, Hinchey discloses stripping an FCS field from the header, recalculating the FCS, and attaching the recalculated FCS to the packet for transmission over the second network (col. 5, lines 1-28). The secondary reference, Mallory, teaches the use of the LARQ protocol in an Ethernet network (col. 4, lines 17-38) and that LARQ headers can contain a FCS field (col. 6, lines 11-15). It is also clear from these and other passages in Mallory (i.e. col. 5, lines 18-23 and col. 6, lines 53-56) that network devices distinguish between LARQ frames and non-LARQ frames. Thus Examiner maintains that it would have been obvious to one of ordinary skill in the art at the time of the invention, in view of all of the above teachings, to perform the steps of claims 1, 3, and 5-8 in order to convert an LARQ Ethernet frame into a conventional Ethernet frame. Since the references provide motivation for the combination, where the second reference is used to supply the motivation, Examiner maintains that the combination is proper.

On pages 8-10 of the Appeal Brief, Applicant argues that "By combining Hinchey with Mallory, the principle of operation of Hinchey would change". Examiner, respectfully, disagrees. As stated earlier, the principle of operation, as cited in Hinchey, is to prepare a first network

packet having a header and an information field for transmission over a second network by removing the header information from the first network packet and associating a second header with the information field of the first packet because this "has the desirable qualities of requiring less computation than complete translation and not increasing the packet size as in encapsulation" (col. 1, line 66-col. 2, line 21). By combining Hinchey with Mallory in order to convert an LARQ Ethernet frame into a conventional Ethernet Frame, the principle of Hinchey is maintained since this process prepares a first network packet (LARQ Ethernet packet) having a header and an information field for transmission over a second network (conventional Ethernet network) by removing the header information from the first network packet (LARQ header), and associating a second header (conventional Ethernet header) with the information field of the first packet. Therefore, Examiner maintains that the combination of Hinchey and Mallory is proper since it does not change the principle of operation of Hinchey.

On pages 10-13 of the Response, Applicant argues that "Hinchey and Mallory, taken singly or in combination, do not teach or suggest" all of the claim limitations as outlined in the Final Rejection. For instance, Applicant argues that Hinchey and Mallory do not teach or suggest "a first logic block for detecting a LARQ header in a frame; a second logic block for stripping the LARQ header and a FCS in the frame; and a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame" in a home phone line network controller. Examiner, respectfully, disagrees. Examiner submits that the phrase "logic block" is very broad and reads on any mechanism to implement the desired step since the mechanism would require logic to perform the step. Examiner also submits that "network controller" is very broad and reads on any mechanism in a network that sends and receives

information on the network since this device, as broadly defined, controls traffic on the network, where Mallory teaches that LARQ is used on phone lines (col. 4, lines 32-38) such that the network controller is, as broadly defined, a "home phone line network controller". Thus, as outlined in the Final Rejection, Hinchey teaches a first logic block for detecting a header in a frame; a second logic block for stripping the header and a FCS in the frame; and a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame (col. 1, line 66-col. 2, line 21 and col. 5, lines 1-28). Mallory teaches that a conventional Ethernet header and an LARQ header differ and that LARQ headers can contain FCS (col. 4, lines 16-38 and col. 6, lines 9-20). Thus, Examiner maintains that Hinchey in view of Mallory discloses "a first logic block for detecting a LARQ header in a frame; a second logic block for stripping the LARQ header and a FCS in the frame; and a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame" in order to convert an LARQ header to a conventional Ethernet header.

Applicant goes on to argue that Hinchey and Mallory do not teach or suggest "wherein an asserted first signal to the first logic block indicates that the LARQ header is enabled and must be stripped from the frame". Examiner, respectfully, disagrees. The first logic block detects the LARQ header in the frame. The above limitation recites that the first logic block receives a signal indicating that the LARQ header is present (enabled) where, since the LARQ header is present, it must be stripped from the frame. Examiner also notes that the above limitation only requires that the logic receive a signal from either itself or another source that indicates that the LARQ header is present. Since the first logic block is used to detect the LARQ header, it is inherent that the first logic block receives a signal that the LARQ header is present when the first

logic block detects the LARQ header. Given the above arguments, and as stated in the Final Rejection, although Hinchey and Mallory do not expressly disclose the "nuts and bolts" of the invention, such as disclosing this signaling, it is nonetheless implicit in the combination of Hinchey and Mallory that such signaling must take place in order to have the first logic block detect the LARQ header.

Applicant further argues that Hinchey and Mallory do not teach or suggest "wherein the first logic block asserts a second signal and a third signal to the second logic block, wherein the second signal indicates that the FCS is to be stripped from the frame, wherein the third signal indicates that the LARQ header is to be stripped from the frame". Again, Examiner, respectfully, disagrees. The above limitation only requires that the mechanism for detecting the LARQ header (first logic block) signals (second and third signals) the mechanism for stripping the information in the header (second logic block) that the present frame contains an LARQ header and an FCS. Again, it is inherent that the mechanism for stripping the information would receive a signal indicating that the information to be stripped is present since the mechanism for stripping the information needs to know that the information is present in order for the stripping can occur. In addition, Mallory discloses that the presence of the FCS is optional (col. 6, lines 9-20) such that the use of two signals, one for stripping the LARQ header and one for stripping the FCS, allows for a stripping of the LARQ header when an FCS is not present. Given the above arguments, and as stated in the Final Rejection, although Hinchey and Mallory do not expressly disclose the "nuts and bolts" of the invention, such as disclosing this signaling, it is nonetheless implicit in the combination of Hinchey and Mallory that such signaling must take place in order to have the second logic block strip the proper fields from the frame.

In addition, Applicant argues that Hinchey and Mallory do not disclose or fairly suggest "wherein an asserted fourth signal to the third logic block enables the recalculation of the FCS". Again, Examiner, respectfully, disagrees. The above limitation only requires that the mechanism for recalculating the FCS (third logic block) receives a signal that enables recalculation of the FCS. Again, it is inherent that the mechanism for recalculating the FCS would need a signal to indicate when recalculation of the FCS should take place. Otherwise the mechanism will not know for which frames the FCS should be recalculated. Given the above arguments, and as stated in the Final Rejection, although Hinchey and Mallory do not expressly disclose the "nuts and bolts" of the invention, such as disclosing this signaling, it is nonetheless implicit in the combination of Hinchey and Mallory that such signaling must take place in order to have the third logic block recalculate the FCS for the proper frame.

On pages 13-17 of the Appeal Brief, Applicant argues that the rejection of claim 2 using Hinchey, Mallory, and Callon is not proper. Examiner agrees and has withdrawn the rejection of claim 2. Claim 2 is currently objected to for the reasons stated above. Therefore, Examiner will not respond to any of the arguments Applicant has made regarding the rejection of claim 2.

On pages 18-21 of the Appeal Brief, Applicant argues that the "Examiner has not presented any objective evidence for combining Hinchey with Mallory and Gibson" since the "Examiner's motivations appear to have been gleaned from the secondary reference (Gibson)". Specifically, Applicant argues that one of ordinary skill in the art would not be motivated to combine a primary reference with secondary references when the primary reference does not contain an explicit motivation for the combination. Examiner disagrees with Applicant's assertion that the motivation provided in the secondary references, Mallory and Gibson, is

insufficient to support a *prima facie* case of obviousness merely because these motivations are found in the secondary rather than the primary reference. Examiner submits that obviousness is not established by determining if one of ordinary skill in the art, after having read the primary reference, would have been motivated to find an additional reference to cure any defects in the primary reference given only the teachings of the primary reference, as Applicant suggests. Rather obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in *the references themselves* (not just the primary reference) or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Since motivation can only be determined "In light of all the evidence" (*In re Fine*), a proper case of *prima facie* obviousness can be made if the motivation is provided in the secondary reference. Since Examiner has focused on the combination of Hinchey and Mallory above, Examiner will rely on these previous arguments to explain the propriety of the Hinchey and Mallory combination. Examiner will proceed by focusing on the combination of Hinchey and Mallory with Gibson. In this case, Examiner submits, as discussed above, that Hinchey and Mallory teach "a home phone line network controller, wherein the home phone line network controller comprises: a first logic block for detecting a LARQ header in a frame, a second logic block for stripping the LARQ header and a FCS in the frame; and a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame" where the LARQ stripping converts an LARQ Ethernet packet into a conventional

Ethernet packet. The secondary reference, Gibson, teaches that, in an Ethernet network (page 1, lines 4-18), Ethernet devices enter sleep mode in order to conserve power where the sleep mode uses a wake pattern in order to wake up a device in sleep mode (page 6, lines 15-22; page 7, lines 14-19; and page 9, line 21-page 12, line 10). Simply put, Gibson teaches transmitting wake patterns, using Ethernet frames, to devices in sleep mode in order for the device to wake up. Thus Examiner maintains that it would have been obvious to one of ordinary skill in the art at the time of the invention, in view of all of the above teachings, to perform the steps of claims 4 and 9-12 in order to convert an LARQ Ethernet frame into a conventional Ethernet frame where the frame contains a wake pattern used to wake up devices that have entered sleep mode. Since the references provide motivation for the combination, where the second reference is used to supply the motivation, Examiner maintains that the combination is proper.

On pages 21-24 of the Appeal Brief, Applicant argues that "Hinchey, Mallory and Gibson, taken singly or in combination, do not teach or suggest" all of the claim limitations as outlined in the Final Rejection. For instance, Applicant argues that Hinchey, Mallory, and Gibson do not teach or suggest "determining if a bit pattern at a set byte location in the stripped frame matches a wake pattern". Examiner, respectfully, disagrees. Examiner submits that the Gibson teaches determining if a bit pattern at a set byte location in a conventional Ethernet frame (page 1, lines 4-18) matches a wake pattern (page 6, lines 15-22; page 7, lines 14-19; and page 9, line 21-page 12, line 10). Hinchey and Mallory teach stripping an LARQ Ethernet frame to form a conventional Ethernet frame, as discussed above. Thus, as outlined in the Final Rejection, Examiner submits that Hinchey in view of Mallory in further view of Gibson teaches

"determining if a bit pattern at a set byte location in the stripped frame matches a wake pattern" in order to wake up a conventional Ethernet device which is in sleep mode.

Applicant further argues that Hinchey, Mallory, and Gibson do not teach or suggest "a home phone line network controller compris[ing]: a first logic block for detecting a LARQ header in a frame; a second logic block for stripping the LARQ header and a FCS in the frame; and a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame". Examiner, respectfully, disagrees. Examiner submits that the phrase "logic block" is very broad and reads on any mechanism used to implement the desired step since the mechanism would require logic to perform the step. Examiner also submits that "network controller" is very broad and reads on any mechanism in a network that sends and receives information on the network since, as broadly defined, this device controls traffic on the network, where Mallory teaches that LARQ is used on phone lines (col. 4, lines 32-38) such that the network controller is, as broadly defined, a "home phone line network controller". Thus, as outlined in the Final Rejection, Hinchey teaches a first logic block for detecting a header in a frame; a second logic block for stripping the header and a FCS in the frame; and a third logic block for recalculating the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame (col. 1, line 66-col. 2, line 21 and col. 5, lines 1-28). Mallory teaches that a conventional Ethernet header and an LARQ header differ and that LARQ headers can contain FCS (col. 4, lines 16-38 and col. 6, lines 9-20). Thus, Examiner maintains that Hinchey in view of Mallory in further view of Gibson discloses "a home phone line network controller compris[ing]: a first logic block for detecting a LARQ header in a frame; a second logic block for stripping the LARQ header and a FCS in the frame; and a third logic block for recalculating

the FCS for the stripped frame and for adding the recalculated FCS to the stripped frame" in order to convert an LARQ header to a conventional Ethernet header.

Applicant goes on to argue that Hinchey, Mallory, and Gibson do not teach or suggest "wherein an asserted first signal to the first logic block indicates that the LARQ header is enabled and must be stripped from the frame". Examiner, respectfully, disagrees. The first logic block detects the LARQ header in the frame. The above limitation recites that the first logic block receives a signal indicating that the LARQ header is present (enabled) where, since the LARQ header is present, it must be stripped from the frame. Examiner also notes that the above limitation only requires that the logic receive a signal from either itself or another source that indicates that the LARQ header is present. Since the first logic block is used to detect the LARQ header, it is inherent that the first logic block receives a signal that the LARQ header is present when the first logic block detects the LARQ header. Given the above arguments, and as stated in the Final Rejection, although Hinchey, Mallory, and Gibson do not expressly disclose the "nuts and bolts" of the invention, such as disclosing this signaling, it is nonetheless implicit in the combination of Hinchey, Mallory, and Gibson that such signaling must take place in order to have the first logic block detect the LARQ header.

Applicant also argues that Hinchey, Mallory, and Gibson do not teach or suggest "wherein the first logic block asserts a second signal and a third signal to the second logic block, wherein the second signal indicates that the FCS is to be stripped from the frame, wherein the third signal indicates that the LARQ header is to be stripped from the frame". Again, Examiner, respectfully, disagrees. The above limitation only requires that the mechanism for detecting the LARQ header (first logic block) signals (second and third signals) the mechanism for stripping

the information in the header (second logic block) that the present frame contains an LARQ header and an FCS. Again, it is inherent that the mechanism for stripping the information would receive a signal indicating that the information to be stripped is present since the mechanism for stripping the information needs to know that the information is present before the stripping can occur. In addition, Mallory discloses that the presence of the FCS is optional (col. 6, lines 9-20) such that the use of two signals, one for stripping the LARQ header and one for stripping the FCS, allows for a stripping of the LARQ header when an FCS is not present. Given the above arguments, and as stated in the Final Rejection, although Hinchey, Mallory, and Gibson do not expressly disclose the "nuts and bolts" of the invention, such as disclosing this signaling, it is nonetheless implicit in the combination of Hinchey, Mallory, and Gibson that such signaling must take place in order to have the second logic block strip the proper fields from the frame.

In addition, Applicant argues that Hinchey, Mallory, and Gibson do not disclose or fairly suggest "wherein an asserted fourth signal to the third logic block enables the recalculation of the FCS". Again, Examiner, respectfully, disagrees. The above limitation only requires that the mechanism for recalculating the FCS (third logic block) receives a signal that enables recalculation of the FCS. Again, it is inherent that the mechanism for recalculating the FCS would need a signal to indicate when recalculation of the FCS should take place. Otherwise the mechanism would not know for which frames the FCS should be recalculated. Given the above arguments, and as stated in the Final Rejection, although Hinchey, Mallory, and Gibson do not expressly disclose the "nuts and bolts" of the invention, such as disclosing this signaling, it is nonetheless implicit in the combination of Hinchey, Mallory, and Gibson that such signaling must take place in order to have the third logic block recalculate the FCS for the proper frame.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Examiner
Art Unit 2665

Daniel J. Ryman DJR 7/9/04
July 9, 2004

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